

**REMARKS**

Claims 77–96 are pending in the present application.

Reconsideration of the claims is respectfully requested.

**35 U.S.C. § 102 (Anticipation)**

Claims 77, 81–90 and 92–96 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 4,841,347 to *Hsu*. This rejection is respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-70 (8<sup>th</sup> ed. rev. 1 February 2003).

Independent claims 77, 93 and 96 each expressly recite that the source/drain portions within the substrate and the source/drain portions on the substrate adjacent the gate electrode together function as a source or drain for the respective device. Such a feature is not depicted or described by the cited reference. *Hsu* teaches a heavily doped epitaxial layer 50 formed over shallow source drain regions 24 and 26 for lowering the sheet resistance of a silicide contact. *Hsu* is silent as to the heavily doped epitaxial regions 50 functioning, together with shallow source drain regions 24 and 26, as source or drain regions for the respective transistor. *Hsu* does not refer to the heavily doped epitaxial regions as source or drain regions or portions thereof. *Hsu* describes the doping of the epitaxial regions as preferably being merely sufficient to reach upwardly diffusing dopants from

shallow source and drain regions 24 and 26, which indicates that the heavily doped epitaxial regions 50 are merely conductive contacts to the shallow source and drain regions 24 and 26.

In addition, independent claim 93 further recites that “insulating material on a bottom and sides of a gate electrode forming a gate oxide between the gate electrode and a source region and between the gate electrode and a drain region.” Thus, claim 93 recites that the oxide on sidewalls of the gate electrode function as a gate oxide between the gate electrode and portions of the source and drain regions beside the gate electrode--that is, the recited doped semiconductor material on the substrate within the opening adjacent to the gate structure and over each of the doped regions within the substrate that form and function, together with the doped regions within the substrate, the source and drain regions for the transistor. Such a feature is not found in the cited reference.

Therefore, the rejection of claims 77, 81–90 and 92–96 under 35 U.S.C. § 102 has been overcome.

**35 U.S.C. § 103 (Obviousness)**

Claims 78–80 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hsu* in view of U.S. Patent No. 5,346,587 to *Doan et al.* This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-123 (8th ed. rev. 1 February 2003). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a *prima facie* case of obviousness, three basic criteria must be met: First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant 's disclosure. MPEP § 2142 at p. 2100-124.

As noted above, independent claim 77, from which the rejected claims depend, recites a limitation not depicted or described by *Hsu*. Such limitation is also not depicted or described by *Doan et al.*

Therefore, the rejection of claims 78–80 under 35 U.S.C. § 103 has been overcome.

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PATENT

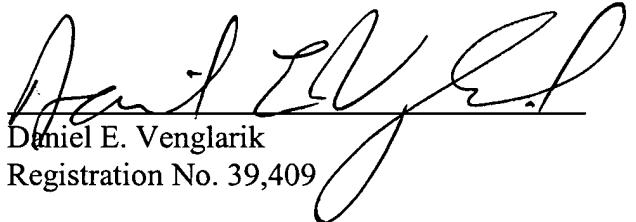
If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at [dvenglarik@davismunck.com](mailto:dvenglarik@davismunck.com).

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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